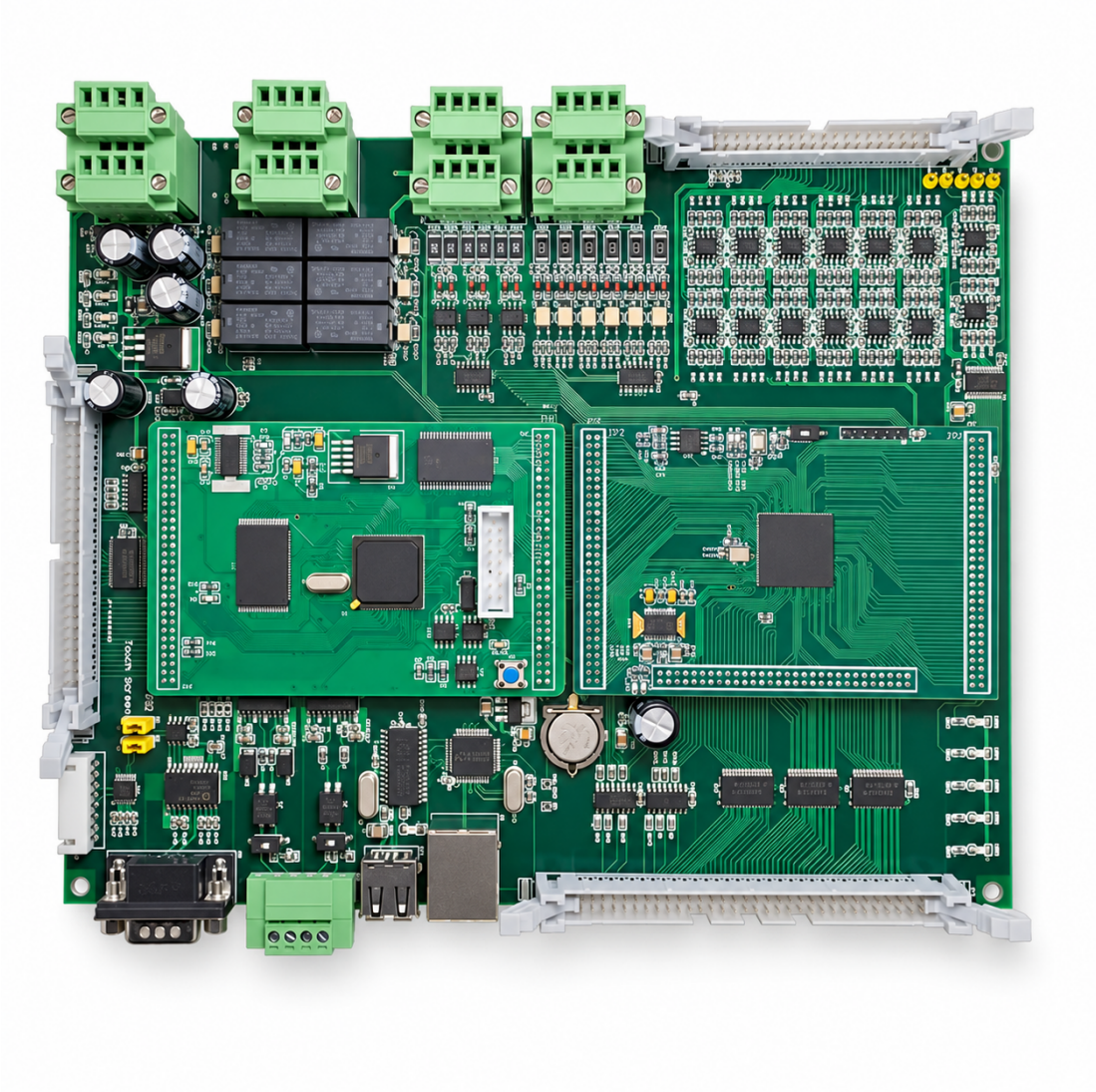
PRODUCT DATASHEET

HDSP-DF28346P DSP + FPGA Industrial Control Board

Dual-core real-time control and data-acquisition platform based on TI Delfino DSP and Xilinx Spartan-6 FPGA



Overview

The HDSP-DF28346P is a modular industrial control platform built around a TI TMS320C28346 DSP core board and a Xilinx Spartan-6 XC6SLX25 FPGA core board. The complete assembly consists of the DSP core board, FPGA core board, and DF industrial-control baseboard. It is intended for power monitoring and acquisition, motor control, modular multilevel converter (MMC) control, medical instrumentation, and industrial automation.

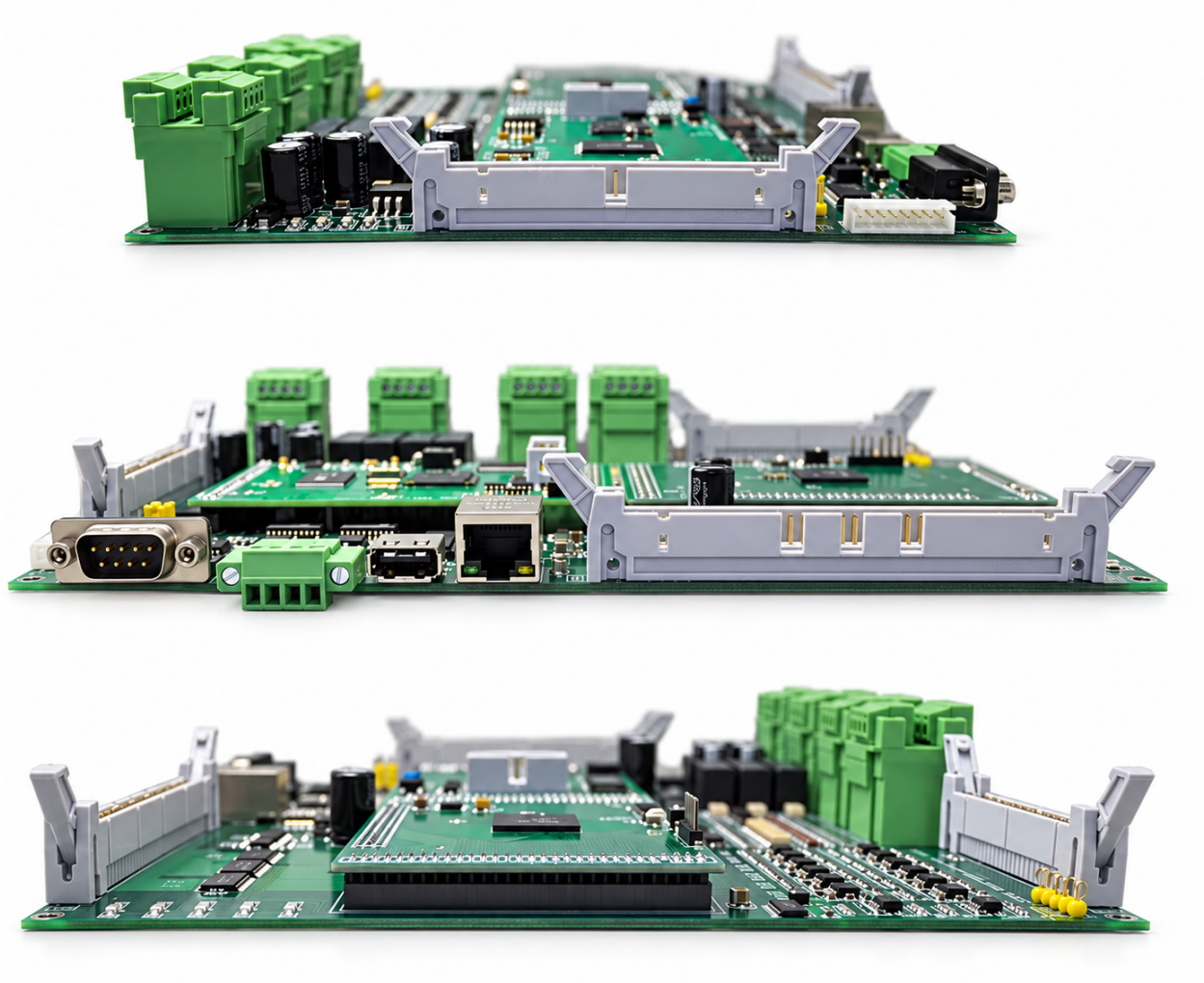
Development focus
The board integrates analog acquisition, high-density PWM, isolated field I/O, serial communications, CAN, and Ethernet so application engineers can concentrate on upper-layer control algorithms and system integration.

Product Configuration

ITEM	DF28335/346	DF28335P/346P
DSP core board	TMS320F28335 or TMS320C28346	TMS320F28335 or TMS320C28346
FPGA core board	Spartan-6 XC6SLX16 or XC6SLX25	Spartan-6 XC6SLX25
PWM	32 channels generated by FPGA	60 total: 12 DSP + 48 FPGA
IGBT fault inputs	Not included	16 total; 12 routed to FPGA
ADC	16 channels, 16-bit, +/-20 V	3 x 8 channels, 16-bit, +/-20 V
DAC	4 channels, 12-bit, +/-10 V	4 channels, 12-bit, +/-10 V
Digital inputs	6 optically isolated channels	6 optically isolated channels
Relay outputs	6 optically isolated channels	6 optically isolated channels
Isolated RS-232 / RS-485 / CAN	Included	Included
Ethernet	10/100 Mbps with embedded TCP/IP stack	10/100 Mbps with embedded TCP/IP stack
USB	No	Yes
RTC	Yes	Yes
JTAG	1 x 14-pin TI Rev B, 2.54 mm pitch	1 x 14-pin TI Rev B, 2.54 mm pitch

HDSP-DF28346P Processing Architecture

PARAMETER	SPECIFICATION
DSP	TI Delfino TMS320C28346 high-performance signal processor
FPGA	Xilinx Spartan-6 XC6SLX25
Board structure	Interchangeable DSP core, FPGA core, and industrial-control baseboard
Display option	7-inch serial HMI, 1024 x 600 resolution, capacitive touch; described as EMC-oriented in the supplied material



Control and Data-Acquisition Resources

PARAMETER	SPECIFICATION
PWM outputs	Up to 60 channels on P variants: 12 from DSP and 48 from FPGA after programming. PWM output-enable pins are provided.
IGBT fault inputs	16 fault-input channels on P variants; 12 are associated with the FPGA. Compatible with 5 V-level IGBT driver fault outputs.
ADC	Three groups of eight 16-bit channels (24 total) on P variants. Analog input range +/-20 V. Sampling can be controlled independently by the FPGA for data-acquisition use.
DAC	4 channels, 12-bit resolution, precision reference source, +/-10 V output range.
Digital / remote inputs	6 optically isolated acquisition channels. 12 V or 24 V input. Minimum stated isolation voltage: 3750 Vrms.
Relay / remote outputs	6 dry-contact relay outputs with optical isolation between control and contact circuits. Minimum stated isolation voltage: 2500 Vrms. Relay contact rated current: 5 A. Source material also states 6 kV impulse withstand.

Communications

PARAMETER	SPECIFICATION
RS-232	Isolated transceiver with integrated isolated DC/DC; common-mode transient immunity >25 kV/us; +/-15 kV ESD protection; up to 460 kbps; 2.5 kVrms signal/data isolation. Optional Modbus RTU software.
RS-485	Isolated transceiver with integrated isolated DC/DC; common-mode transient immunity >25 kV/us; +/-15 kV ESD protection; up to 500 kbps; 2.5 kVrms isolation; common-mode interference suppression and configurable jumper termination. Optional Modbus RTU software.
CAN	Isolated CAN transceiver with integrated isolated DC/DC; common-mode transient immunity >25 kV/us; +/-15 kV ESD protection; up to 1 Mbps; 2.5 kVrms isolation; common-mode interference suppression and configurable filter/termination network.
Ethernet	10/100 Mbps Ethernet with embedded TCP/IP stack. Protocol support stated in the source: IPv4, DHCP, ARP, ICMP, IGMP, UDP, and TCP. Optional Modbus TCP, online update, and Ethernet waveform-recording software.

Development Header / Signal Groups

NO.	SIGNAL GROUP
1	LED
2	FPWM
3	EPWM
4	ADC
5	DA
6	FAULT
7	DI
8	DO
9	RS232
10	RS485-TX
11	RS485-RX
12	CAN-TX
13	CAN-RX
14	NET-SERVER

Optional Power Supply

The supplied materials describe an optional industrial control power supply with short-circuit, overload, and overvoltage protection. Rated outputs are shown below. The 24 V input and each output rail are described as isolated, supporting the IGBT-driver, voltage/current Hall-sensor, and other isolated-power loads.

PARAMETER	SPECIFICATION
Input	24 VDC
Output rail 1	+5 V / 4 A
Output rail 2	+15 V / 2 A
Output rail 3	-15 V / 1 A
Output rail 4	+24 V / 1 A

Optional Software Packages

PARAMETER	SPECIFICATION
Power-electronics algorithms	Park transform, Clarke transform, three-phase phase-locked loop, PI controller, capacitor-based AC-voltage hardware PLL, PWM rectifier control, three-level SVPWM, and three-level FSVPWM control.
Low-level / driver examples	External EEPROM control, real-time clock control, acquisition and calculation, digital input/output control, CAN communication, Modbus RTU, Modbus TCP, real-time waveform recording, fault waveform recording, and NTC temperature calculation.

Typical Applications

PARAMETER	SPECIFICATION
Power systems	Power monitoring, signal acquisition, and power-electronics control
Motion control	Motor drives and real-time motor-control development
Converters	Modular multilevel converter (MMC) and multilevel PWM control
Instrumentation	Medical instruments and multi-channel data acquisition
Automation	Industrial field control and automation equipment

Integration and Safety Notes

Engineering validation required
Pin assignments, connector orientation, power-up sequence, grounding, isolation barriers, output-contact ratings, and software compatibility must be confirmed against the delivered hardware and official schematics before deployment. Mechanical dimensions were not stated in the supplied materials and are therefore not specified in this document.

Use current-limited bench supplies during first power-up. Verify all supply rails before installing the DSP and FPGA core boards. Maintain the intended isolation boundaries and do not apply field voltage until the applicable channel type and polarity have been confirmed. Provide suitable enclosure, airflow, strain relief, fusing, and protective earth arrangements for the final system.

Document basis: compiled and translated from the product images and downloaded web-page content supplied by the user. Specifications are presented as source-derived information, not as independent certification.